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Heavy-Ion-Induced Snapback in CMOS Devices

R. KOGA and W. A. KOLASINSKI
Space Sciences Laboratory
Laboratory Operations
The Aerospace Corporation
El Segundo, CA 90245-4691

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Los Angeles Air Force Base
P.O. Box 92960
Los Angeles, CA 90009-2960

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TYRON FISHER, LT, USAF
MOIE Project Officer
SSD/CLPO

JONATHAN EMMES, MAJ, USAF
MOIE Program Manager
AFSTC/WCO OL-AB

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Single-event snapback (SES) susceptibilities of selected complementary metal-oxide semiconductor (CMOS) devices to heavy ions were measured, first using N, Ne, Ar, Cu, and Kr ion beams. Like latchup, snapback was observed macroscopically by detecting the abnormally high bias current condition. However, the snapback susceptibility characteristics differed from those of latchup, and consequently we could unambiguously measure the snapback responses. The responses are expressed in terms of the cross section for varying bias and the stopping power of ions. Test data indicate that CMOS devices with rather long channel lengths (on the order of 3 μm) are free from SES when operated at about 5 V. However, present-day theories have predicted that this regenerative breakdown mode of upset may become very important at 5 V or below for devices with extremely short n-channel lengths.

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Preface

We would like to thank our Aerospace colleagues Bob Walter, Sam Imamoto, John Elder, Brad Johnson, and Jon Osborn for their generous assistance in the development of the instrumentation. Our thanks are also due to the members of the Lawrence Berkeley Laboratory 88-in. cyclotron staff for beam delivery.

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I. Introduction

Snapback has been investigated for over a decade in the area of the avalanche breakdown study in short-channel n-channel metal-oxide semiconductor (NMOS) transistors [1],[2]. (The term snapback first appeared in the literature in 1978 [2] and has been in common usage since then [3],[4]. Previous studies have concluded that n-channel metal-oxide semiconductor field effect transistors (MOSFETs) may undergo a stable, regenerative breakdown, which results in an abrupt increase of the drain-source current. This mode of breakdown occurs when a parasitic three-layer transistor (sometimes referred to as a parasitic bipolar device) is activated by deposition of a charge at the sensitive area (see section IV). The charge may be deposited through ionization [e.g., single-event snapback (SES)] or through avalanching (e.g., over-voltage stress condition at a signal node). Another result of these studies is that snapback can be induced more readily for devices with a short channel length.

The typical snapback drain I-V characteristic curve resembles that of latchup [an activation of parasitic signal-to-clutter ratio (SCR) circuits][3]. Even though the mechanism of snapback differs from that of latchup, our detection techniques are very similar. Therefore, it is informative to compare the two mechanisms and to point out ways to distinguish them. The comparison is shown in Table 1. As can be seen in the last item in the table, snapback in a CMOS inverter can be terminated (stopped) by switching the logic level of the inverter. We have adapted this method to ensure that we are measuring snapback, not latchup.

Table 1. Comparison of Snapback and Latchup in CMOS Devices

Item of Comparison	Snapback	Latchup
Induced current-carrying path	Parasitic 3-layer bipolar transistor circuit	Parasitic 4-layer SCR circuit
Typical location of path in a CMOS inverter circuit	From source of n-channel to drain of same channel	From source of p-channel to source of n-channel
Magnitude of current measured at bias pins	On the order of 100 mA	On the order of 100 mA
Method of terminating high current condition	Shut off power supply and restart, or Change input polarity of inverter	Shut off power supply and restart

For the present study, we decided to test five device types of the Harris radiation hardened CMOS family: HS54C138RH (three to eight decoder), HS82C08RH (bus transceiver), HS3374RH (eight-bit level converter), HS81C55RH [256 x 8 static random access memory (SRAM)], and HS80C85RH (eight-bit microprocessor). All device types were manufactured with a thin epitaxial layer. Therefore, we expected that the probability of observing latchup was low. Nevertheless, it was still necessary to utilize the items in Table 1 to distinguish SES from latchup.

These devices have been fabricated to operate with the bias voltage ranging from about 4 to 11 V (see earlier device specifications), although recent manufacturer specifications limit the pow-

er supply voltage to a region between 4.75 and 5.25 V. An exception is HS3374RH, which is still rated to 11 V. Because all these device types function well at higher supply voltages, they have been operated above 9 V in some space applications. These applications demand higher throughputs, which can be achieved only at a higher supply voltage. The present study of snapback was initiated to set a limit on the maximum supply voltage at which SES susceptibility is still acceptably low, since we inferred from earlier studies that the snapback sustaining voltage of these devices would most likely be higher than 5 V [3],[4].

II. Test Methods

The tests were carried out at the Lawrence Berkeley Laboratory 88-in. cyclotron. The ion beam delivery, analysis, and exposure techniques are identical to those used for other single-event upset testing and therefore can be found in previously published technical literature [5].

Since the occurrence of snapback is accompanied by a dramatic increase in the device bias current, local heating is inevitable. It is therefore mandatory that the snapback be detected and cleared before the device has a chance to heat up. We used a circuit that performed the functions of sensing (within the order of 1 μs), clearing (within the order of 1 ms), and recording snapback (in a few milliseconds). For details of the circuit, the reader is referred to the description of the same circuit used to detect latchup [6].

All irradiations were carried out on biased devices. In one set of tests, all input pins were held at either a high or low logic level throughout the irradiation. We call this the static test. In another set, we varied the inputs (raised to V_{DD}, reduced to V_{SS}, and repeated at 1 MHz) and also applied 1 MHz clock pulses if applicable. This is considered the active test. Both static and active tests were needed to measure the dynamic properties of snapback, as discussed below.

We did not know the number of off-state n-channel transistors in each device during the test. Since SES occurs only at the off-state transistors, we at first thought that we should take into account the number of these transistors. However, we later concluded that the number of off-state transistors is reasonably constant under test conditions. The main reason is that a basic CMOS memory cell has at least two n-channel transistors, one of which was always turned off, independent of the logic state. Nevertheless, by avoiding unusual biasing conditions, we created a reasonably well-balanced testing situation. For example, we set four inputs to "high" and the other four inputs to "low" for an eight-bit device.

The bias voltage was varied by 1/4 V, starting from the maximum voltage of 11 V. Only at the threshold region was a finer separation of voltage steps used.

III. Test Results and Comments

The test results follow.

1. HS54C138RH: Figure 1 shows the cross sections from the static test of a single device [serial no. (S/N) 337] at various voltage levels and with several ion species. Similar curves from another device (S/N 353) are shown in Figure 2. Figure 3 shows the combined test data of several devices, including S/Ns 337 and 353. The linear energy transfer (LET) vs cross section at any voltage can be extracted from the figure. We also combined the static test results of several devices to produce the bands of data shown in Figure 4. All other figures that describe test results were produced in this fashion, except Figure 10.

2. HS3374RH: A composite of several devices produced curves for the static tests, as shown in Figure 5. During the active tests, we obtained the composite curves shown in Figure 6.

3. HS81C55RH: The composite graphs of the static and the active tests are shown in Figures 7 and 8, respectively.

4. HS82C08RH: For this device type only, both the static and the active test results were very similar. Consequently, we combined all data for this device type, as shown in Figure 9.

5. HS80C85RH: The most dramatic change in the snapback cross section as a consequence of applying clock pulses occurred in this device type. From the static test, we observed a large cross section (Figure 10), while no snapback was detected during the active tests. We took a few more data points during the static/active test of another HS80C85RH. Since the data points were not numerous enough to complete a cross-section curve, we have shown the results of only one device.

We noticed that for the most part: (a) the cross section was higher for the static test, (b) cutoff voltage (above 9 V) was normally independent of the input activity, and (c) HS80C85RH was drastically different from the other devices, as shown in Table 2.

Table 2. Static vs Active Test Results

	Effects of Applying Clock Pulses		
Device Type	**Cross Section**	**Threshold Voltage**	**Cutoff Voltage**
HS54C138RH	High for static tests at higher LET About the same at lower LET	About the same for most of the beam	9.2
HS3374RH	High for static tests	About the same	10.1
HS81C55RH	High for static tests at higher LET About the same at lower LET	Just about the same	9.8
HS82C08RH	About the same	Just about the same	9.6
HS80C85RH	Very high for static tests	Very high for active tests	9.3 for static tests >11.0 for active tests

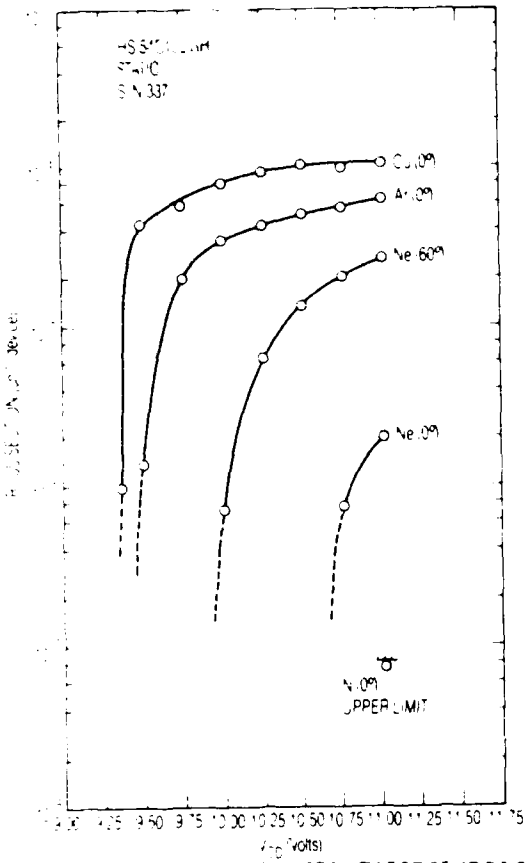

Figure 1. Static Test Results for HS54C138RH (S/N 337)

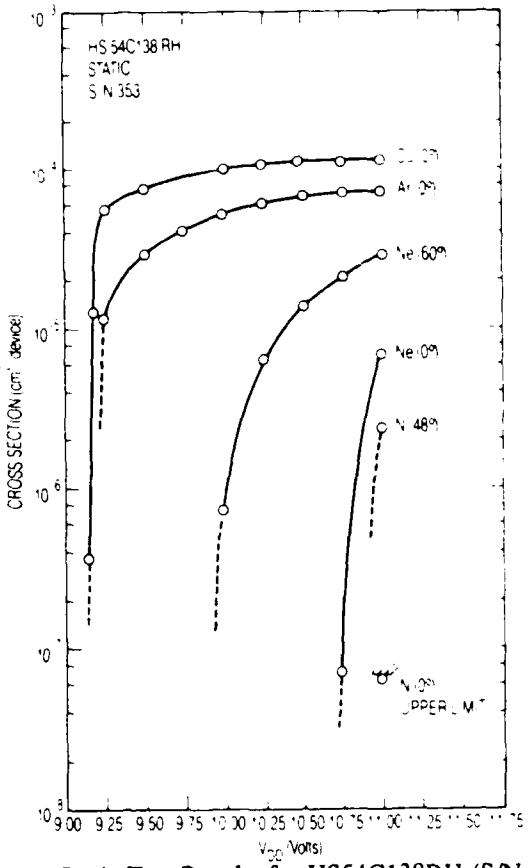

Figure 2. Static Test Results for HS54C138RH (S/N 353)

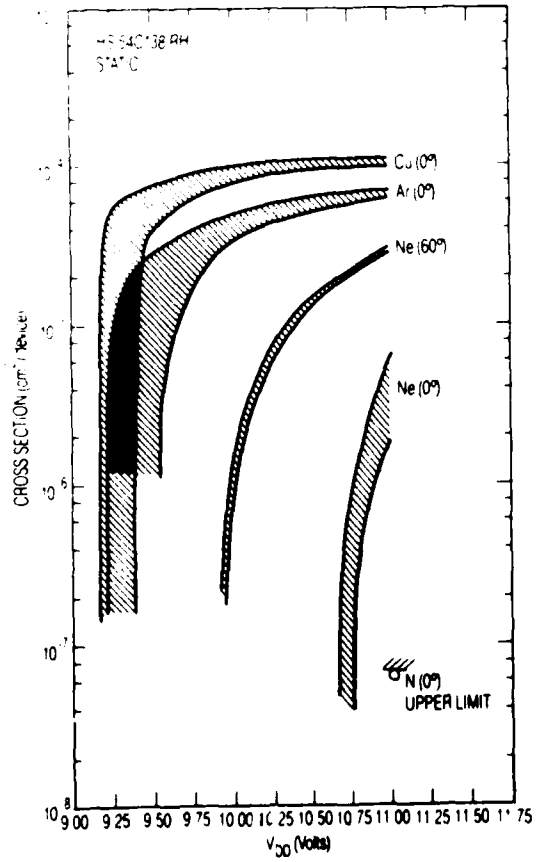

Figure 3. Static Test Results for HS54C138RH (Combined)

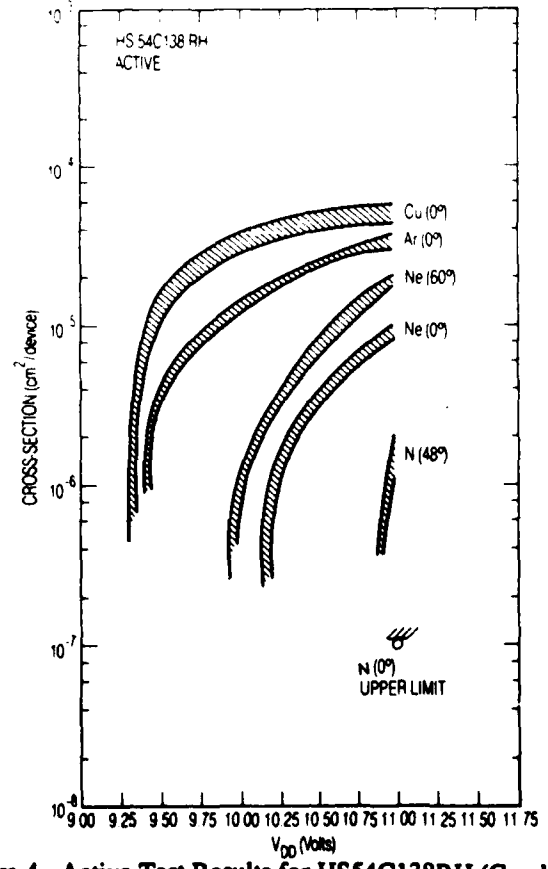

Figure 4. Active Test Results for HS54C138RH (Combined)

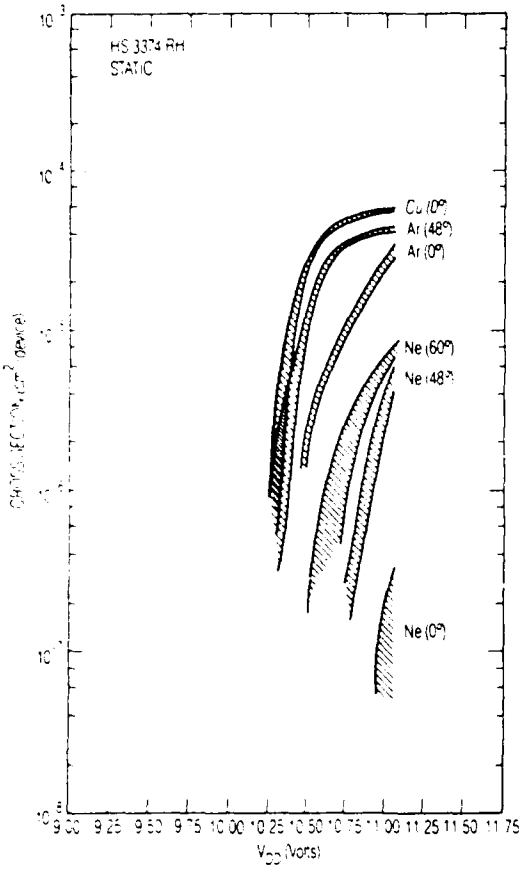

Figure 5. Static Test Results for HS3374RH (Combined)

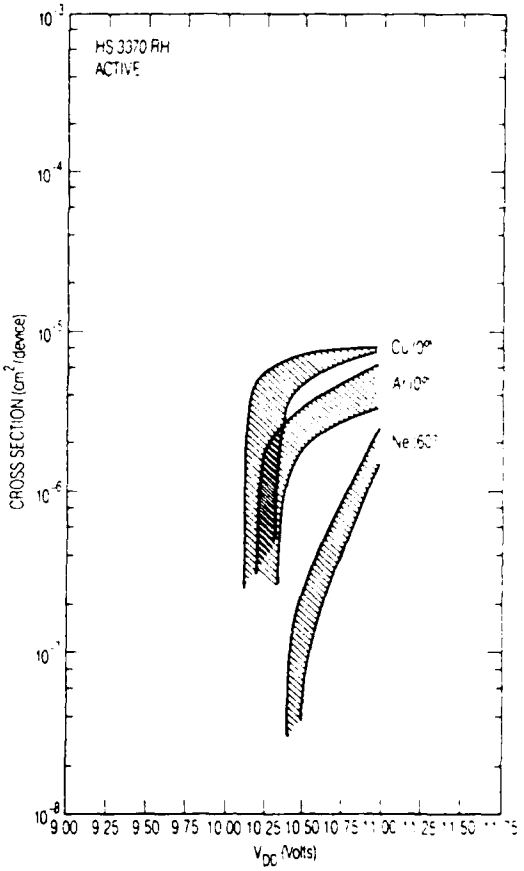

Figure 6. Active Test Results for HS3374RH (Combined)

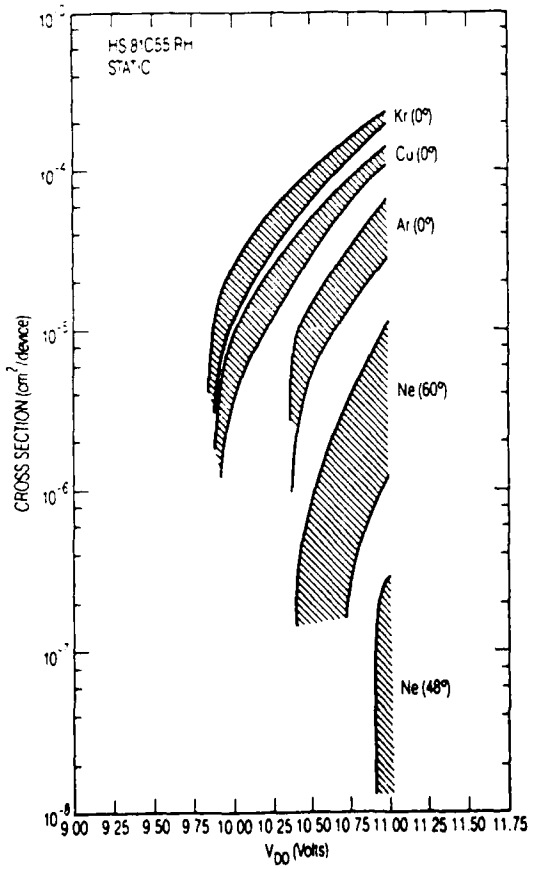

Figure 7. Static Test Results for HS81C55RH (Combined)

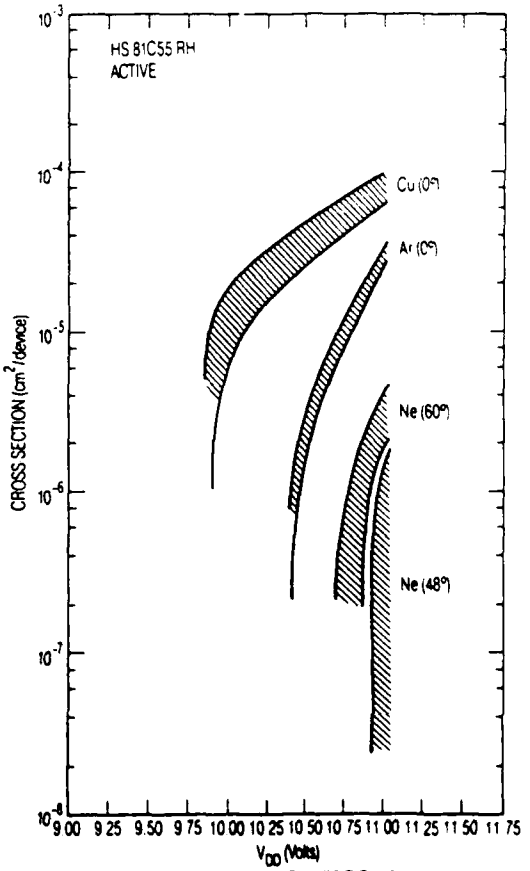

Figure 8. Active Test Results for HS81C55RH (Combined)

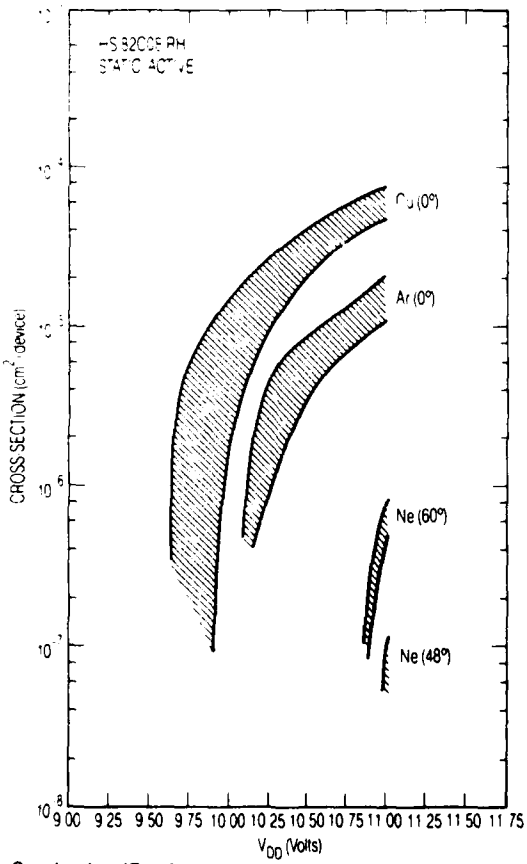

Figure 9. Active/Static Test Results for HS82C08RH (Combined)

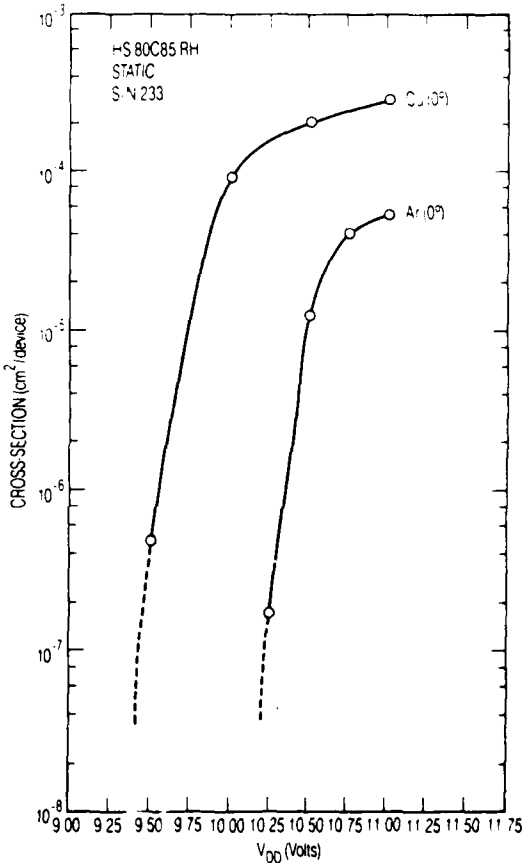

Figure 10. Static Test Results for HS80C85RH (S/N 233)

The snapback cross section increased with increasing bias voltage. At a lower voltage, there is an abrupt cutoff in the cross section curve (a sharp knee). The above characteristics are not often shared by a latchup whose cross section tends to decrease more smoothly when the bias voltage is reduced (e.g., latchup observed for TC5564 8K x 8 SRAM). However, we do not have enough data to make a definitive conclusion, and therefore, the shapes of the curves have not been used to distinguish snapback from latchup.

IV. Snapback Model

Previous studies have advanced a semiqualitative model of snapback [3],[4]. Even though the model has not been developed specifically for heavy-ion-induced snapback, heavy ions have been included in the set of possible causes. Therefore, we will briefly summarize Beitman's basic snapback model in order to qualitatively explain SES [4]. All device types have the epitaxial n-layer on the highly doped n^+ material. Since the off-state NMOS transistors are responsible for the snapback in a CMOS circuit, we expect a well-developed depletion region around the drain, as shown in Figure 11a. Soon after the passage of an ion through the depletion region, the electron-hole pairs commence movement along the field lines. Most electrons travel toward the drain, whereas the holes move mainly toward the source (Figure 11b). Some holes, however, travel through the p-regions toward the ground plane. At this stage, the parasitic bipolar transistor can be turned on, as shown in Figure 11c. Once the parasitic transistor is turned on and the regenerative breakdown condition has occurred, the transistor can be shut off only when the current between the drain and the source is reduced below the cutoff (sustaining) current level. The effect of funnelling may accelerate the onset of the snapback. The introduction of the p-well feature slightly complicates the picture, since additional parasitic (vertical) bipolar transistors become active. Nevertheless, the basic model describes the main snapback mechanism, i.e., a low resistance path is formed between the source and the drain of the off-state NMOS transistor.

With the aid of the basic model, it is easy to see that there are two ways to remove the snapback. One is to shut off the device power and restart. This works for any n-channel device. The other way, which is applicable to CMOS devices only, involves shutting off the accompanying p-channel transistor by reversing the state of the logical bit. This action stops the current flow through the n-channel, and hence removal of the snapback condition results. Therefore, in some CMOS devices, a heavy-ion-induced snapback may be difficult to observe, especially when the logic states of the bits in the device are being altered quickly and continuously.

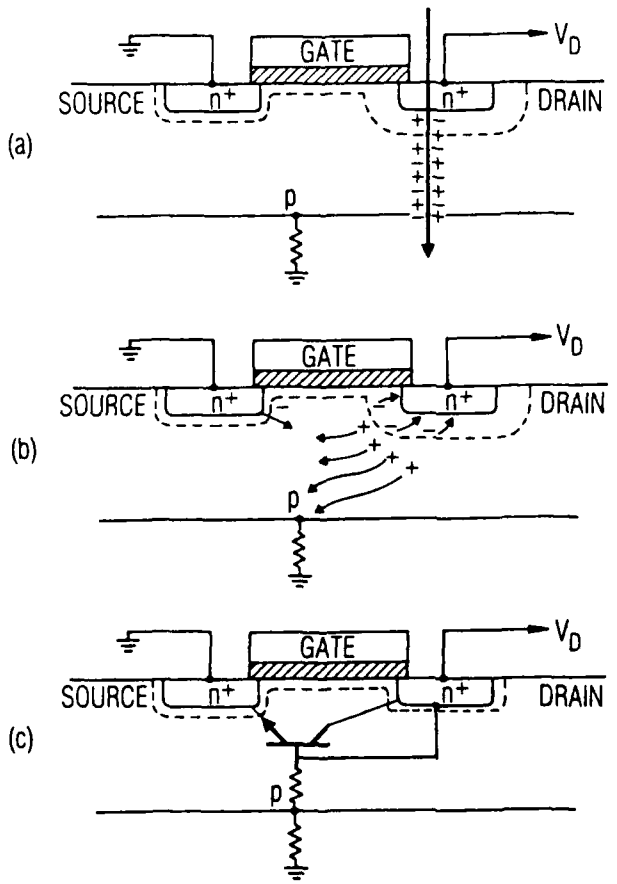

Figure 11. Heavy-Ion-Induced Snapback. (a) Ion injection into depletion region, (b) movement of electrons and holes, (c) formation of parasitic bipolar transistor.

V. Discussion

The highest cross section of the devices at the bias of 11 V is compared with the physical die size in Table 3. The ratios in the table seem to indicate that the sensitive n-channel depletion regions of each device type amount to only a small section of the die at this bias. Therefore, not all n-channel regions are vulnerable. However, the present data are not sufficient to state that either (1) snapback occurs only in a limited region of a die (e.g., buffers) or (2) snapback occurs in a small region at this level of LET (and is presumed to increase to all n-channel regions at higher LET). In either case, in the space environment, these devices will not experience snapback in a much wider area than we have measured.

Table 3. Maximum (Static) Cross Section vs Die Size

Device Type	Cross Section, cm^2	Die Size, cm^2	Ratio
HS54C138RH	1.1 E-4	3.0 E-2	0.004
HS3374RH	6.0 E-5	4.2 E-2	0.002
HS81C55RH	2.4 E-4	2.8 E-1	0.001
HS82C08RH	7.5 E-5	3.0 E-2	0.003
HS80C85RH	3.0 E-4	2.8 E-1	0.001

The best indicator that we have measured snapback (not latchup) comes from the observed influence of clock pulses on the cross section. Since previous studies had presented a good understanding of snapback, we were able to follow various manifestations of SES as we proceeded with testing [3]. The application of square wave clock pulses (1 MHz) at the inputs generally reduced the cross section. However, there was no effect on HS82C08RH. We believe that major portions of the circuits of this device type were never driven by the input clock pulses. On the other hand, all vulnerable transistors in HS80C85RH seemed to have responded to the clock pulses, preventing the appearance of the snapback state in the external area. Within the limited time available for testing, we did not use all combinations of instructions for HS80C85RH. However, we did not find any instruction that produced snapback.

We did not observe any permanent damage in the devices when they were functionally tested after the SES testing. Since the snapback bias current can exceed 100 mA, we assume that metal fusing or melting can occur if the snapback is unchecked. It appears that our tester detected and terminated snapback quickly enough to mitigate any possible damage.

Increased bias voltage reduces the propagation delay of CMOS devices. Therefore, in applications where speed is important, devices may be operated at higher voltages. However, at 10 V (for example), the device may experience a snapback in space. Moreover, we currently do not have a proper method to assess the snapback rate. A precise model of SES, which expresses such parameters as the size of the sensitive region, needs to be completed before the computer code can be developed for the snapback rate calculation.

VI. Conclusions

The channel length of the tested devices is on the order of 3 μm. For these devices, a heavy-ion-induced snapback will not occur as long as the device bias is set at (or below) 9 V. However, according to present-day theory, the onset of snapback will move toward a lower bias level for devices of shorter channel lengths [2],[4]. Therefore, SES susceptibility is yet another factor that should be taken into consideration by device manufacturers as the miniaturization of space-borne microcircuits continues in the CMOS and NMOS technologies. We hope to extend our investigation by selecting test samples with much shorter channel lengths in the near future.

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